UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/541,857	04/03/2000	James Digby Collier	491.039US1	4161

21186 7590 10/13/2005

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH
1600 TCF TOWER
121 SOUTH EIGHT STREET
MINNEAPOLIS, MN 55402

EXAMINER	
LAM, TUAN THIEU	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 10/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/541,857	COLLIER ET AL.
	Examiner	Art Unit
	Tuan T. Lam	2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *59-88* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *59-88* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 September 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the amendment filed 9/6/2005. Claims 59-88 are pending and are under examination.

Drawings

1. The drawings were received on 9/6/2005. These drawings are acceptable.

Specification

1. The disclosure is objected to because of the following informalities: the brief description of the drawings in pages 3 and 4 of the specification fails to include a brief description of figure 1c filed on 9/6/2005.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 59-70, 72-73, 75-82 and 84-85 are rejected under 35 U.S.C. 102(b) as being anticipated by Kouno (JP 60-224319).

Figure 9 of Kouno shows a frequency divider circuit comprising a first signal means (not shown) for generating a first periodic signal (CL1) to be frequency divided by the frequency divider, said frequency divider comprises an input terminal for receiving the first periodic signal, an even number of amplifier stages (two amplifier stages 6-8; 9-11) connected in series, with an

output of a last amplifier stage (9-11) connected to input of a first amplifier stage (6-8) and each amplifier each having an associated propagation delay and a transistor (7-8; 9-11) coupled between a supply terminal Vdd and a reference terminal (VSS) for modulating delay through the associated amplifier, the first periodic signal (CL1) applied to the first input terminal to a control electrode of the transistor of the odd amplifier stage (6-8), and for applying the second clock signal (CL2) to a control electrode of said transistor of the even amplifier (9-11) to modulate the propagation delays through the associated amplifier stages about half the period of said first and second periodic signals so that when the propagation delay through the even amplifier stage (9-11) decreases, the propagation delay through the odd amplifier stage increases, and an output terminal (Q, Q/) for outputting a generated frequency divided signal, although, the first and second generating means are not shown, the transistors of the frequency divider are capable of receiving analog period signals so that not fully open and fully closed but to act as variable resistance, wherein each of the transistor of each odd amplifier stage (transistors receiving clock signal CL1) that is used to modulate the propagation delay through the odd amplifier stage references the first periodic signal to a voltage supply and each of the transistors (transistors receiving clock signal CL2) of each of even amplifier stage that is used to modulate the propagation delay through the even amplifier stage references the second periodic signal to the same voltage supply (figure 5 of Kouno shows the first and second periodic clock signals CL and CL/ swing between VDD and VSS, thus, the periodic clock signals are referenced to a same supply voltage VDD) as called for in claims 59, 75, 84 and 85.

1. Regarding claim 60, the number of amplifiers is two.

2. Regarding claim 61, Kouno shows a single frequency divider. However, it is known and obvious to one skilled in the art to cascade a plurality of Kouno et al.'s frequency divider to obtain a desired frequency divided signal. Therefore, the limitation of cascading a plurality of frequency dividers will not be patentable under 35USC 103(a).

3. Regarding claims 62 and 76, each amplifier stage 6-8; 9-11 comprises differential amplifier.

4. Regarding claim 63, logic circuitry includes said transistor in each amplifier stage is seen as transistors in boxes 7, 8 and 10, 11.

5. Regarding claims 64, 77 and 79, each amplifier stage of Kouno inherently has hysteresis characteristics which varies in response to the clock signals.

6. Regarding claim 78, the limitations recited therein is inherently present in Kouno.

7. Regarding claims 65-67 and 80-81 each amplifier stage is CMOS.

8. Regarding claims 68 and 69, said first transistors are seen as transistors in boxes 7-8 for the odd stage 6-8, and for the even stage 242, said second transistors are seen as the transistors in boxes 10, 11. Said first and second transistors are coupled in series between the supply terminal and the reference terminal.

9. Regarding claims 70 and 82, Kouno does not specifically indicate the periodic signal (CLOCK) in a range of 100 Mhz. However, it is known that CMOS technology is capable of operating with frequencies of 100 Mhz or higher. Therefore, the limitation of using the clock signal at 100 Mhz is seen to be inherently presently in Kouno's frequency divider.

10. Regarding claim 72, first and second inverters are seen as transistors 6 and 9.

11. Regarding claim 73, N channel transistors are seen as transistors in boxes 7, 8, 10, 11.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 74 is rejected under 35USC 103(a) as being unpatentable over Kouno (JP 60-224319). The Kouno reference discloses all the aspects of the present invention as noted above except Kouno does not disclose the size of n channel controlling transistors (7, 8) is larger than the size of n channel transistors (the n channel transistors of the inverters in boxes 6). However, it is notoriously well known to implement the n channel controlling transistors with a larger size in order to reset the crossed inverters (6; 9) at a quicker speed thus preventing an erroneous operation. Therefore, the limitation of having n channel controlling transistor at a larger size than the size of the n channel inverting transistors will not be patentable under 35USC 103(a).

12. Claims 71 and 83 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kouno (JP 60-224319) in view of Maemura (USP 5,172,400). The Kouno reference discloses all the aspects of the present invention as noted above except logic circuitry connected in series between at least two of the amplifier stages in order to enable division by ratios other than simple powers of two as called for in claims 71 and 83. Figure 15 of Maemura reference teaches the use of a logic circuitry (41) implemented in between two amplifier stage to obtain a division ratio other

than power of two. Therefore, it would have been obvious to a person skilled in the art at the time of the invention was made to include the logic circuitry (41) of Maemura in the circuit arrangement of Kouno's figure 9 for the flexibility of obtaining a frequency divided output other than power of two.

13. Claims 87 and 88 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kouno (JP 60-224319). The Kouno reference discloses all the aspects of the present invention as noted above except Kouno does not disclose first and second generating means formed by a single circuit as called for in claims 87 and 88. Although, the first and second generating means are not shown inn Konno, the transistors of the frequency divider are capable of receiving analog period signals so that not fully open and fully closed but to act as variable resistance. It is obvious to one skilled in art to form the first and second generating circuits in one single circuit in order to save space on an integrated chip and to reduce manufacturing cost. Therefore, outside of an non-obvious results the obviousness of forming the first and second generating circuit on a single circuit to save space on an integrated chip and to reduce manufacturing cost will not be patentable under 35USC 103(a).

Claim Rejections - 35 USC § 103

4. Claims 59-70, 72-82 and 84 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murray (USP 4,845,727), prior art of record, in view of Weste and Eshraghian (Weste et al.), Principles of CMOS VLSI Design, second edition, Fig. 5.55b, pages 328, 1993, newly cited prior art.

Figure 5 of Murray shows a signal generating circuit comprising a first signal means (not shown) for generating a first periodic signal (3) to be frequency divided by the frequency divider, said frequency divider comprises an input terminal for receiving the first periodic signal, a second signal means (5) for generating a second periodic signal which is anti-phase with the first periodic signal, an even number of amplifier stages (two amplifier stages 1, 2) connected in series, with an output of a last amplifier stage (2) connected to input of a first amplifier stage (1).

The Murray reference does not show the detailed structure of the first and second amplifier stage wherein each amplifier each having an associated propagation delay and a transistor coupled between a supply terminal and a reference terminal for modulating delay through the associated amplifier, the first periodic signal applied to the first input terminal to a control electrode of the transistor of the odd amplifier stage and for applying the second clock signal to a control electrode of said transistor of the even amplifier to modulate the propagation delays through the associated amplifier stages about half the period of said first and second periodic signals so that when the propagation delay through the even amplifier stage decreases, the propagation delay through the odd amplifier stage increases, and an output terminal for outputting a generated frequency divided signal, wherein said first and second generating means are arranged to generate the respective first and second periodic signal as analogue periodic signals having an amplitude which causes said transistors to be fully open or closed but to act as variable resistances, and wherein each of the transistor of each odd amplifier stage that is used to modulate the propagation delay through the odd amplifier stage references the first periodic signal to a voltage supply and each of the transistors of each of even amplifier stage that is used

to modulate the propagation delay through the even amplifier stage references the second periodic signal to the same voltage supply as called for in claims 59, 75, 84 and 85.

Figure 5 of Weste et al. shows a detailed structure of a D flip flop having all the limitations that Murray's D flip flop (amplifier stage) does not specifically show. Weste et al.'s D flip flop is simple having only eight transistors. Therefore, it would have been obvious to person skilled in the art at the time of the invention was made to use Weste's D flip flop circuits in place of Murray's flip flop circuits 1 and 2 because Weste et al.'s flip flop circuits occupy less space on a chip.

Regarding the limitation of "first and second periodic signals as analogue periodic signals having an amplitude which causes said transistors to be not fully open or fully closed but to act as variable resistance", the transistors (transistors receiving clock signals CLOCK) of Weste is capable of receiving analogue periodic signals having an amplitude which causes said transistors to be not fully open or fully closed but to act as variable resistance.

Regarding claim 61, figure 5 of Murray shows a single frequency divider. However, it is known and obvious to one skilled in the art to cascade a plurality of Murray et al.'s frequency divider to obtain a desired frequency divided signal. Therefore, the limitation of cascading a plurality of frequency dividers will not be patentable under 35USC 103(a).

Regarding claims 62 and 76, each amplifier stage of Weste et al. comprises differential amplifier.

Regarding claim 63, logic circuitry includes said transistor in each amplifier stage is seen as transistors receiving DATA, DATA_BAR, CLOCK and CLOCk_BAR as shown Weste et al. reference.

Regarding claims 64, 77 and 79, each amplifier stage of Weste et al. reference inherently has hysteresis characteristics which varies in response to the clock signals.

Regarding claim 78, the limitations recited therein is inherently present in Weste et al. reference.

Regarding claims 65-67 and 80-81 each amplifier stage of Weste et al. is CMOS.

Regarding claims 68 and 69, said first transistors are seen as transistors receiving DATA, DATA_BAR, CLOCK and CLOCk_BAR as shown Weste et al. reference. Said first and second transistors are coupled in series between the supply terminal and the reference terminal.

Regarding claims 70 and 82, Weste et al. reference does not specifically indicate the periodic signal (CLOCK) in a range of 100 Mhz. However, it is known that CMOS technology is capable of operating with frequencies of 100 Mhz or higher. Therefore, the limitation of using the clock signal at 100 Mhz is seen to be inherently presently in Weste et al.'s frequency divider.

Regarding claim 72, first and second inverters are seen as cross-coupled inverters of Weste et al. reference.

Regarding claim 73, N channel transistors are seen as transistors receiving DATA, DATA_BAR, CLOCK and CLOCk_BAR as shown Weste et al. reference.

Regarding claim 74, the combination of Murray and Weste et al. references discloses all the aspects of the present invention as noted above except Weste et al. does not disclose the size

of n channel controlling transistors (transistors receiving clock signal CLK) is larger than the size of n channel transistors (the n channel transistors of the cross-coupled inverters). However, it is notoriously well known to implement the n channel controlling transistors with a larger size in order to reset the cross-coupled inverters at a quicker speed thus preventing an erroneous operation. Therefore, the limitation of having n channel controlling transistor at a larger size than the size of the n channel inverting transistors will not be patentable under 35USC 103(a).

5. Claims 71 and 83 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murray (USP 4,845,727) in view of Weste et al. and in further view of Maemura (USP 5,172,400).

The combination of Murray and Weste et al. references discloses all the aspects of the present invention as noted above except logic circuitry connected in series between at least two of the amplifier stages in order to enable division by ratios other than simple powers of two as called for in claims 71 and 83. Figure 15 of Maemura reference teaches the use of a logic circuitry (41) implemented in between two amplifier stage to obtain a division ratio other than power of two. Therefore, it would have been obvious to a person skilled in the art at the time of the invention was made to include the logic circuitry (41) of Maemura in the circuit arrangement of the combined Murray and Weste et al. references for the flexibility of obtaining a frequency divided output other than power of two.

6. Claims 87 and 88 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murray (USP 4,845,727) in view of Weste et al.

The combination of Murray and Weste et al. references discloses all the aspects of the present invention as noted above except the combination of Murray and Weste et al. references does not disclose first and second generating means formed by a single circuit as called for in

claims 87 and 88. Although, the first and second generating means are not shown in Murray, the transistors of the frequency divider are capable of receiving analog period signals so that not fully open and fully closed but to act as variable resistance. It is obvious to one skilled in art to form the first and second generating circuits in one single circuit in order to save space on an integrated chip and to reduce manufacturing cost. Therefore, outside of an non-obvious results the obviousness of forming the first and second generating circuit on a single circuit to save space on an integrated chip and to reduce manufacturing cost will not be patentable under 35USC 103(a).

Response to Arguments

7. Applicant's arguments filed 09/06/2005 have been fully considered but they are not persuasive.

35 USC 102(b):

Regarding the rejection of claims 59-70, 72-73, 75-82 and 84-85 under 35USC 102(b) as being anticipated by Kouno (JP 60-224319), applicant argues that Kouno reference fails to show "wherein said first and second generating means arranged to generate the respective first and second periodic signals as analogue periodic signals having an amplitude which causes said transistors to be not fully open or fully closed but to act as variable resistance" as called for in claims 59, 75, 84 and 85. The Examiner respectfully disagrees. As stated in the rejection, the Examiner's position is that since Kouno's frequency divider has essentially the same structure as shown in applicant's figure 1c (and all of the claimed structure and function set forth in the

claims 59, 75, 84 and 85 is fully anticipated), the figure 9 circuit of Kouno is clearly capable of "receiving analog periodic signals so that not fully open and fully closed but to act as variable resistance" (i.e., the recited intended use of applicant's inventive circuit). Furthermore, because applicant has failed to provide any evidence or support showing that Kouno's circuit is not capable of receiving analog periodic signals so that not fully open and fully closed but to act as variable resistance, the rejection is maintained.

Applicant argues that page 5 of Kouno stating "the transfer clock signal (CL1) is 'H,' the switching circuit (8) made up of a NMOS transistor is turned ON and forcibly become 'L' (Vss level)", thus, teach away from operating these transistors in a manner so that they act as variable resistors as recited in claims 59, 75, 84 and 85 is not persuasive. The passage that the applicant mentioned is a description of Kouno's circuit operating with square clock signals. It is no where in the reference conclusively suggesting that the circuit is not capable of receiving analog periodic signals so that not fully open and fully closed but to act as variable resistance. Again, applicant has failed to provide any evidence or support showing that Kouno's circuit is not capable of receiving analog periodic signals so that not fully open and fully closed but to act as variable resistance, the rejection is maintained.

Claims 60-70, 72-73 and 76-82, depending on claims 59 and 75, remain rejected for the reasons of the independent claims 59 and 75.

35USC 103(a):

Claims 71, 74, 83, 87 and 88 remain rejected under 35USC 103(a) for the reasons of the independent claims 59, 75, 84 and 85.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Lam whose telephone number is 571-272-1744. The examiner can normally be reached on Monday to Friday (7:30 am to 6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY P. CALLAHAN can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan T. Lam
Primary Examiner
Art Unit 2816

10/04/2005

IN THE DRAWINGS

Please amend the drawings as follows:

In FIG. 1A, reference number "10" is amended to "10a."

Add new FIG. 1C.

Approved T. Lam 9/04/05

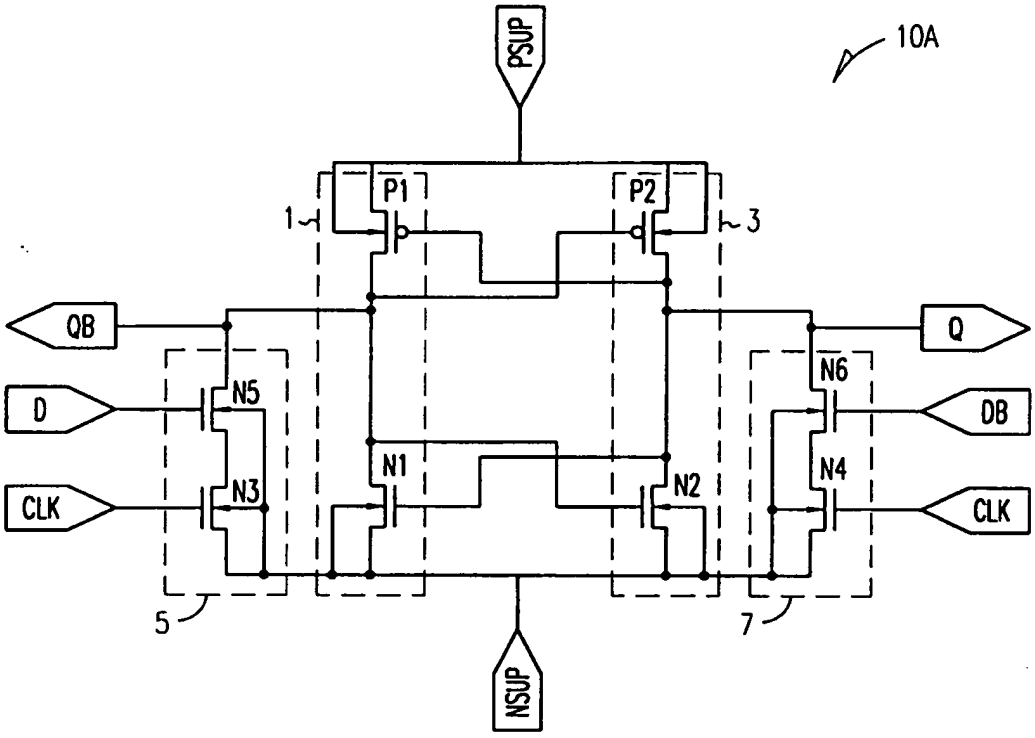

FIG. 1A

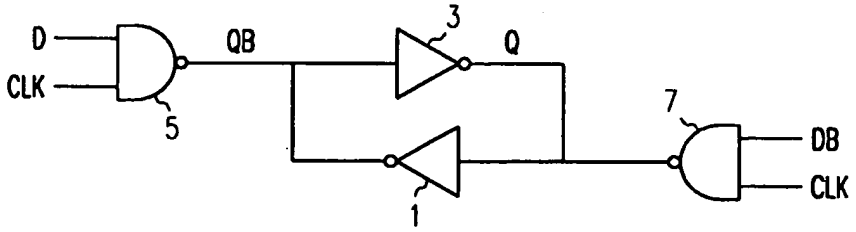

FIG. 1B

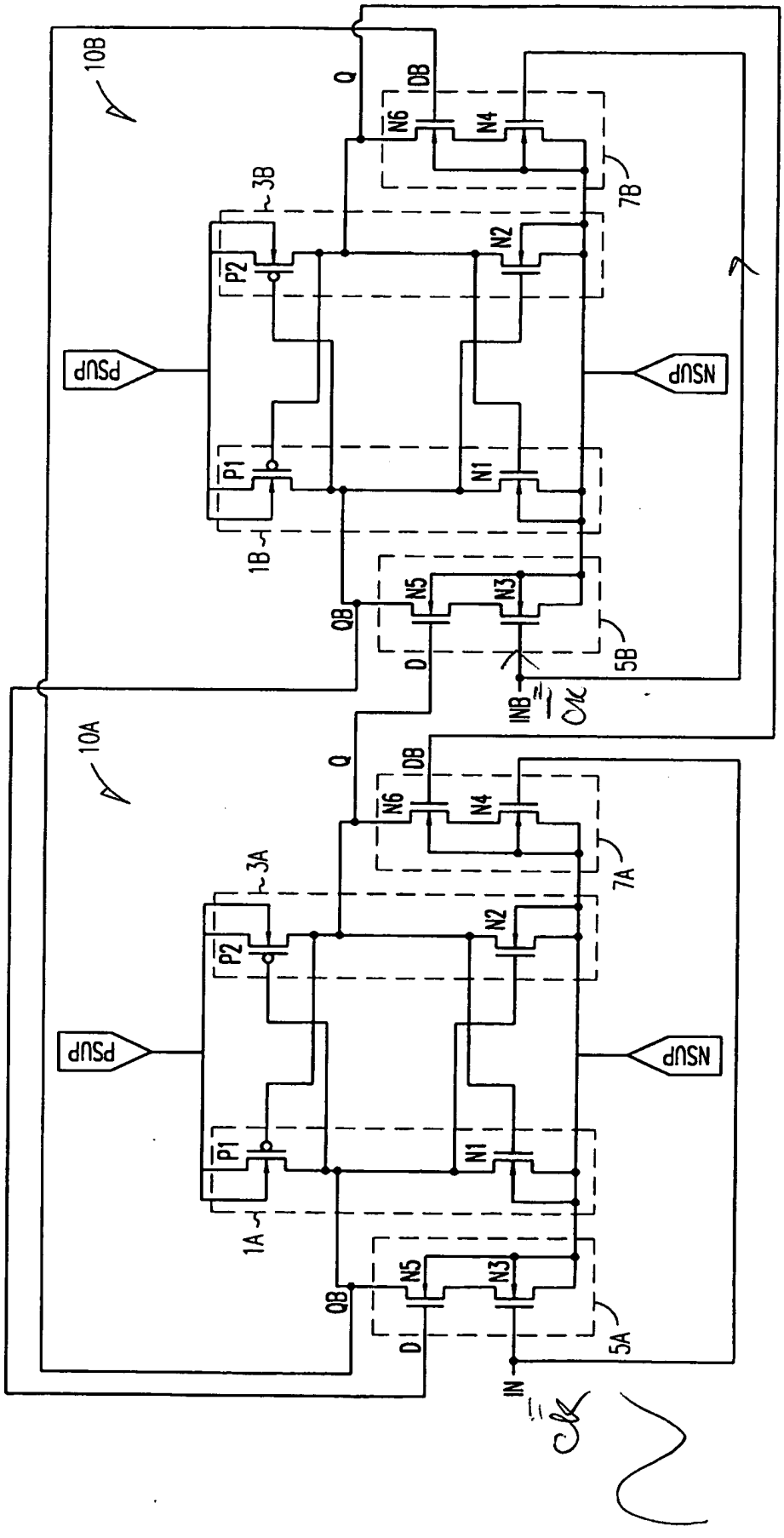

FIG. 1C